Amendments to The Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

What is claimed is:

1. (Original): A method for controlling a plurality of I/O devices being attached to a microprocessor by a special number and type of interfaces comprising:

connecting a configurable chip to the I/O space of said microprocessor, said configurable chip having a switch matrix;

initializing said I/O devices; and

assigning to said switch matrix, said special number and type of interfaces to each I/O device during said initialization.

2-7 canceled

8. (Original): The method according to claim 1, wherein said switch matrix is adapted to assign I/O pins according to the needs of each I/O device.

9. (Original): The method according to claim 1 further comprising switching in hardware using ID bits on each I/O device.

10-57 Canceled

58. (New): A method for configuring a controller capable of supporting a plurality of communication protocols, the method comprising:

accessing an I/O device value;

determining from the accessed I/O device value, one of a plurality of communications protocols supported by the controller for devices attached to the controller;

configuring the configurable I/O signal pins of the controller to provide one or more signal paths from the controller to one or more corresponding attached devices, each signal path comprising a group of one or more I/O signal pins of the configurable I/O signal pins, the signal paths adapted to the determined communications protocol; and

the controller communicating to the one or more corresponding attached devices using the determined communications protocol by way of the one or more signal paths.

59. (New): The method according to claim 58 wherein the controller is adapted to support a plurality of protocols, the protocols having corresponding groups of I/O signal pin configurations.

60. (New): The method according to claim 58 wherein the controller comprises a microprocessor, the microprocessor performing the step of accessing the I/O device value.

61. (New): The method according to claim 58 wherein the controller accesses the I/O device value from an SEEPROM via IIC protocol.

62. (New): The method according to claim 58 wherein the I/O device value is packaged with one or more of the attached I/O devices.

63. (New): The method according to claim 58 wherein the controller comprises a plurality of working units, one working unit for each I/O bus protocol of the plurality of I/O bus protocols wherein the step of configuring the signal pins comprises the further steps of:

selecting a first working unit of the plurality of working units, the first working unit adapted to performing the first protocol; and

providing a path from the first working unit to the signal I/O pins via a switch matrix of the controller.

64. (New): The method according to claim 63 comprising the further steps of:

providing information based on the I/O device value to the switch matrix, the switch matrix providing one or more communication paths for each of the plurality of working units to the interface; and

based on the information provided, selecting the switch matrix paths of the first working unit for communication with the first I/O device.

65. (New): The method according to claim 63, wherein the plurality of communications protocols consist of any one of IIC bus (I^2C), Universal Asynchronous Receiver/Transmitter (UART), USB, PCI, Firewire, TCPIP or General Purpose I/O (GPI/O) protocols.

66. (New): The method according to claim 58 wherein the groups of one or more I/O signal pins of the determined communications protocol comprise I/O signal pins of one or more other communications protocols supported by the controller.

67. (New): The method according to claim 58 comprising the further steps of:

accessing a second I/O device value;

determining from the accessed second I/O device value, a second communications protocol of the plurality of communications protocols supported by the controller for devices attached to the controller;

configuring configurable I/O signal pins of the controller to provide one or more second signal paths from the controller to one or more corresponding attached devices, the signal paths adapted to the determined communications protocol; and

the controller communicating to the one or more corresponding attached devices using the determined second communications protocol.

68. (New): The method according to claim 58 comprising the further step of:

hot-plug attaching one of the devices to the controller.

69. (New): The method according to 68 comprising the further step of:

when the device is hot-plugged attached to the controller, signaling a microprocessor via a microprocessor interrupt signal.

70. (New): A computer program product for configuring a controller capable of supporting a plurality of communication protocols, the computer program product comprising:

a storage medium readable by a processing circuit and storing instructions for execution by a processing circuit for performing a method comprising the steps of:

accessing an I/O device value;

determining from the accessed I/O device value, one of a plurality of communications protocols supported by the controller for devices attached to the controller;

configuring the configurable I/O signal pins of the controller to provide one or more signal paths from the controller to one or more corresponding attached devices, each signal path comprising a group of one or more I/O signal pins of the configurable I/O signal pins, the signal paths adapted to the determined communications protocol; and

the controller communicating to the one or more corresponding attached devices using the determined communications protocol by way of the one or more signal paths.

71. (New): The method according to claim 70 wherein the controller is adapted to support a plurality of protocols, the protocols having corresponding groups of I/O signal pin configurations.

72. (New): The method according to claim 70 wherein the controller comprises a microprocessor, the microprocessor performing the step of accessing the I/O device value.

73. (New): The method according to claim 70 wherein the controller accesses the I/O device value from an SEEPROM via IIC protocol.

74. (New): The method according to claim 70 wherein the I/O device value is packaged with one or more of the attached I/O devices.

75. (New): The method according to claim 70 wherein the controller comprises a plurality of working units, one working unit for each I/O bus protocol of the plurality of I/O bus protocols wherein the step of configuring the signal pins comprises the further steps of:

selecting a first working unit of the plurality of working units, the first working unit adapted to performing the first protocol; and

providing a path from the first working unit to the signal I/O pins via a switch matrix of the controller.

76. (New): The method according to claim 75 comprising the further steps of:

providing information based on the I/O device value to the switch matrix, the switch matrix providing one or more communication paths for each of the plurality of working units to the interface; and

based on the information provided, selecting the switch matrix paths of the first working unit for communication with the first I/O device.

77. (New): The method according to claim 75, wherein the plurality of communications protocols consist of any one of IIC bus (I^2C), Universal Asynchronous Receiver/Transmitter (UART), USB, PCI, Firewire, TCPIP or General Purpose I/O (GPI/O) protocols.

78. (New): The method according to claim 70 wherein the groups of one or more I/O signal pins of the determined communications protocol comprise I/O signal pins of one or more other communications protocols supported by the controller.

79. (New): The method according to claim 70 comprising the further steps of:

accessing a second I/O device value;

determining from the accessed second I/O device value, a second communications protocol of the plurality of communications protocols supported by the controller for devices attached to the controller;

configuring configurable I/O signal pins of the controller to provide one or more second signal paths from the controller to one or more corresponding attached devices, the signal paths adapted to the determined communications protocol; and

the controller communicating to the one or more corresponding attached devices using the determined second communications protocol.

80. (New): The method according to claim 70 comprising the further step of:

hot-plug attaching one of the devices to the controller.

81. (New): The method according to 80 comprising the further step of:

when the device is hot-plugged attached to the controller, signaling a microprocessor via a microprocessor interrupt signal.

82. (New): A system for configuring a controller capable of supporting a plurality of communication protocols, the system comprising:

a network;

a controller system connected to the network, the system comprising a controller, the controller comprising a plurality of configurable I/O signal pins for communicating with one or more I/O devices, wherein the controller system includes instructions to execute a method comprising the steps of:

accessing an I/O device value;

determining from the accessed I/O device value, one of a plurality of communications protocols supported by the controller for devices attached to the controller;

configuring the configurable I/O signal pins of the controller to provide one or more signal paths from the controller to one or more corresponding attached devices, each signal path comprising a group of one or more I/O signal pins of the configurable I/O signal pins, the signal paths adapted to the determined communications protocol; and

the controller communicating to the one or more corresponding attached devices using the determined communications protocol by way of the one or more signal paths.

83. (New): The method according to claim 82 wherein the controller is adapted to support a plurality of protocols, the protocols having corresponding groups of I/O signal pin configurations.

84. (New): The method according to claim 82 wherein the controller comprises a microprocessor, the microprocessor performing the step of accessing the I/O device value.

85. (New): The method according to claim 82 wherein the controller accesses the I/O device value from an SEEPROM via IIC protocol.

86. (New): The method according to claim 82 wherein the I/O device value is packaged with one or more of the attached I/O devices.

87. (New): The method according to claim 82 wherein the controller comprises a plurality of working units, one working unit for each I/O bus protocol of the plurality of I/O bus protocols wherein the step of configuring the signal pins comprises the further steps of:

selecting a first working unit of the plurality of working units, the first working unit adapted to performing the first protocol; and

providing a path from the first working unit to the signal I/O pins via a switch matrix of the controller.

88. (New): The method according to claim 87 comprising the further steps of:

providing information based on the I/O device value to the switch matrix, the switch matrix providing one or more communication paths for each of the plurality of working units to the interface; and

based on the information provided, selecting the switch matrix paths of the first working unit for communication with the first I/O device.

89. (New): The method according to claim 87, wherein the plurality of communications protocols consist of any one of IIC bus (I^2C), Universal Asynchronous Receiver/Transmitter (UART), USB, PCI, Firewire, TCPIP or General Purpose I/O (GPI/O) protocols.

90. (New): The method according to claim 82 wherein the groups of one or more I/O signal pins of the determined communications protocol comprise I/O signal pins of one or more other communications protocols supported by the controller.

91. (New): The method according to claim 82 comprising the further steps of:

accessing a second I/O device value;

determining from the accessed second I/O device value, a second communications protocol of the plurality of communications protocols supported by the controller for devices attached to the controller;

configuring configurable I/O signal pins of the controller to provide one or more second signal paths from the controller to one or more corresponding attached devices, the signal paths adapted to the determined communications protocol; and

the controller communicating to the one or more corresponding attached devices using the determined second communications protocol.

92. (New): The method according to claim 82 comprising the further step of:

hot-plug attaching one of the devices to the controller.

93. (New): The method according to 92 comprising the further step of:

when the device is hot-plugged attached to the controller, signaling a microprocessor via a microprocessor interrupt signal.